

FIG. 1A
(PRIOR ART)

12

CHANNEL
 ~ 30

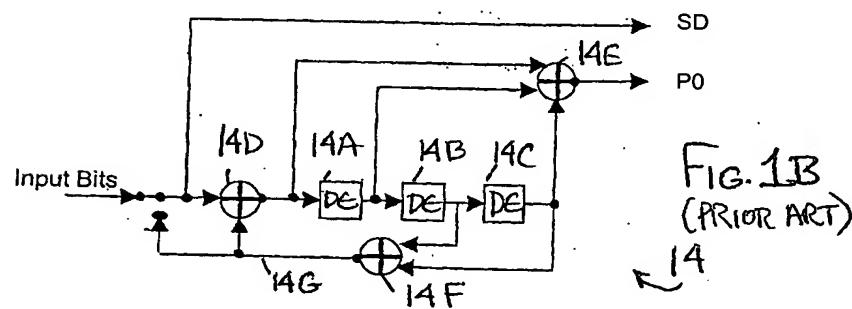


FIG. 1B
(PRIOR ART)

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Input bit	Present encoder state	Next encoder state	State transition	Parity bit
0	000 (0)	000 (0)	$0 \leftrightarrow 0$	0
1	000 (0)	100 (4)	$0 \leftrightarrow 4$	1
0	001 (1)	100 (4)	$1 \leftrightarrow 4$	0
1	001 (1)	000 (0)	$1 \leftrightarrow 0$	1
0	010 (2)	101 (5)	$2 \leftrightarrow 5$	1
1	010 (2)	001 (1)	$2 \leftrightarrow 1$	0
0	011 (3)	001 (1)	$3 \leftrightarrow 1$	1
1	011 (3)	101 (5)	$3 \leftrightarrow 5$	0
0	100 (4)	010 (2)	$4 \leftrightarrow 2$	1
1	100 (4)	110 (6)	$4 \leftrightarrow 6$	0
0	101 (5)	110 (6)	$5 \leftrightarrow 6$	1
1	101 (5)	010 (2)	$5 \leftrightarrow 2$	0
0	110 (6)	111 (7)	$6 \leftrightarrow 7$	0
1	110 (6)	011 (3)	$6 \leftrightarrow 3$	1
0	111 (7)	011 (3)	$7 \leftrightarrow 3$	0
1	111 (7)	111 (7)	$7 \leftrightarrow 7$	1

FIG. 1C
(PRIOR ART)

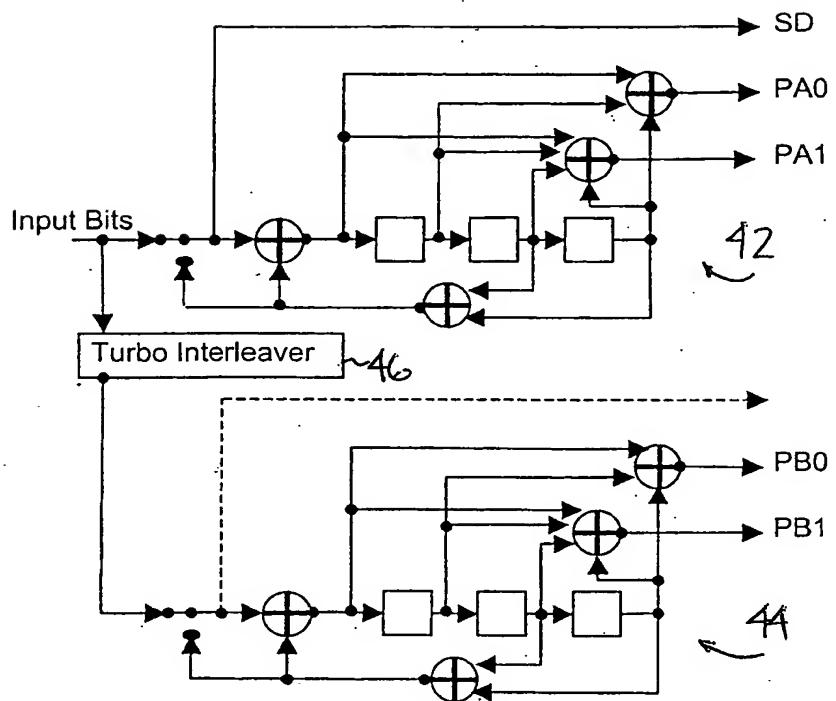


FIG. 2
40
42
(PRIOR ART)

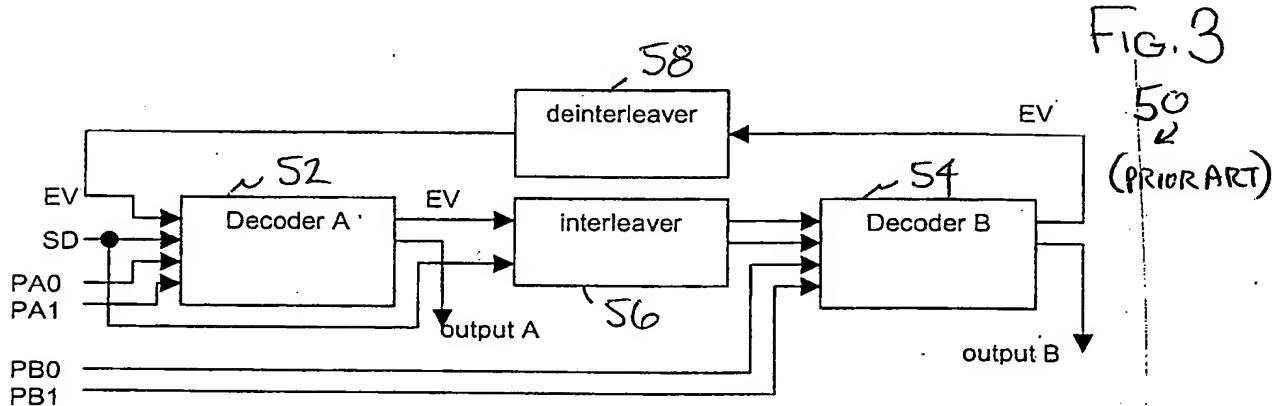


FIG. 3
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(PRIOR ART)

